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10/530,268	04/05/2005	William A. Steer	92781-253537	4632

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EXAMINER	
CHOWDHURY, AFROZA Y	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/530,268	STEER, WILLIAM A.	
	Examiner	Art Unit	
	AFROZA Y. CHOWDHURY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 11-17* is/are rejected.

7)☐ Claim(s) *7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on **May 13, 2008** has been entered. Claims 1-17 are currently pending. Applicant's amended claims are addressed herein below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, and 11-17 are rejected under 35 U.S.C. 102(b) as being unpatentable by **Holloman** (US Patent 6,288,696).

As to claim 1, Holloman discloses an active matrix electroluminescent display device comprising an array of display pixels (fig. 3), each pixel comprising:

an electroluminescent (EL) display element (fig. 1(100));

a drive transistor (fig. 1(28)) for driving a current through the display element (fig. 1(100));

a current sampling resistor (fig. 1(30)),

wherein the EL display element (fig. 1(100)), the drive transistor (fig. 1(28)) and the current sampling resistor (fig. 1(30)) are in series between first and second power lines (abstract, figs. 1, 2, col. 5, lines 38-51); and

circuitry (fig. 1, 2) for providing a feedback signal or signals representing the voltage drop across the current sampling resistor (fig. 1(30)) to at least one feedback line (abstract, col. 2, line 63 – col. 3, line 5),

wherein the display device further comprises processing means for processing pixel drive signals in dependence on the feedback signal or signals (fig. 3, 5, col. 4, lines 54-65).

As to claim 2, Holloman teaches a device where the circuitry for providing a feedback signal or signals comprises a first sampling transistor (fig. 1(32)) connected between one terminal of the current sampling resistor (fig. 1(30)) and a first feedback line (fig. 1, col. 3, lines 6-9).

As to claim 11, Holloman teaches a method of addressing an active matrix electroluminescent display device comprising an array of display pixels, in which each pixel comprises an electroluminescent (EL) display element (fig. 1(100)),

a drive transistor (fig. 1(28)) for driving a current through the display element (fig. 1(100)) and

a current sampling resistor (fig. 1(30)) in series with the EL display element (fig. 1(100)) and the drive transistor (fig. 1(28)), the method comprising, for each pixel:

applying a drive signal (col. 2, line 63 – col. 3, line 5) to the pixel representing a desired current (fig. 1(100));

obtaining a feedback signal representing the current flowing through the display element (fig. 1(100)) by sampling a voltage on the terminals of the resistor (fig. 1(30)) in series with the EL display element (fig. 1(100), col. 2, line 63 – col. 3, line 5, col. 5, lines 38-51); and

using the drive signal and the feedback signal to generate a modified pixel drive signal such that the current flowing is equal to the desired current (col. 2, line 63 – col. 3, line 5, col. 3, lines 19-25).

As to claim 12, Holloman teaches a method wherein using the drive signal and the feedback signal comprises differentially amplifying the signals (figs. 1, 2).

As to claim 13, Holloman discloses a method where sampling a voltage on the terminals of the resistor (fig. 1(30)) in series with the EL display element comprises tapping the voltage from each terminal to a differential amplifier (fig. 1).

As to claim 14, Holloman teaches a method wherein sampling a voltage on the terminals of a resistor in series with the EL display element comprises tapping the voltage from one terminal, the voltage on the other terminal comprising a known supply voltage (figs. 1-3).

As to claim 15, Holloman discloses a method of addressing an active matrix electroluminescent display device comprising an array of display pixels, in which each pixel comprises an electroluminescent (EL) display element (fig. 1(100)),

a drive transistor (fig. 1(28)) for driving a current through the display element (fig. 1(100)) and

a current sampling resistor (fig. 1(30)) in series with the EL display element (fig. 1(100)) and the drive transistor (fig. 1(28)), the method comprising, for each pixel:

driving a desired current through the current sampling resistor (fig. 1(30)) and not through the display element (fig. 1(30));

obtaining a feedback signal representing the corresponding voltage drop across the current sampling resistor (col. 2, line 63 – col. 3, line 5);

storing the feedback signal (col. 2, line 63 – col. 3, line 9); and

using the stored feedback signal as a feedback control signal for subsequently driving current through the display element by applying a voltage to the gate of the drive transistor, the feedback control signal being used to determine the gate voltage (figs. 1, 2, col. 2, line 63 – col. 3, line 5, col. 5, lines 38-51).

As to claim 16, Holloman teaches a method wherein using the stored feedback signal comprises applying the stored feedback signal and a second feedback signal during driving of the display element to a differential amplifier (fig. 1), and using the differential amplifier output to control the drive transistor (fig. 1(28)).

As to claim 17, Holloman teaches a method where the second feedback signal is obtained by sampling a voltage on the terminals of the current sampling resistor (fig. 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Holloman** (US Patent 6,288,696).

As to claim 3, Holloman discloses a device wherein the circuitry for providing a feedback signal or signals comprises a second sampling transistor (figs. 1, 2).

Holloman does not explicitly teach a device wherein the circuitry for providing a feedback signal or signals further comprises a second sampling transistor connected between the other terminal of the current sampling resistor and a second feedback line.

However, it would be obvious to make a display device where the circuitry for providing a feedback signal or signals comprises a second sampling transistor connected between the other terminal of the current sampling resistor and a second feedback line in order to improve circuit operation.

As to claim 4, Holloman teaches a device where each pixel further comprises an address transistor, connected between a data input line and the gate of the drive transistor and wherein the gates of the address transistor (fig. 1(12)) and the or each sampling transistor (fig. 1(32)) are controlled by a shared address line (figs. 1, 2).

As to claim 5, Holloman teaches a device wherein each pixel further comprises a second address transistor wherein the second address transistor is connected between the one terminal of the current sampling resistor and a current drain line (fig. 1).

As to claim 6, Holloman teaches a device wherein the second address transistor is controlled by the shared address line (fig. 1).

Allowable Subject Matter

6. Claims 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claim 7, prior art does not show, "**a second amplifier which receives the output dependent on the current flowing through the current sampling resistor and the pixel drive signal and provides a modified pixel drive signal**" in combination with other limitations of claim 7.

As to claim 8, prior art does not show, "**a sample and hold circuit for holding the output value, and a second amplifier for receiving the held output value and the output dependent on the current flowing through the current sampling resistor**" in combination with other limitations of claim 8.

As to claim 9, prior art does not show, "**a sample and hold circuit for holding the output value, and a second amplifier for receiving the held output value and the output dependent on the current flowing through the current sampling resistor, wherein the data input line is switchable between a power supply line voltage and the output of the second amplifier**" in combination with other limitations of claim 9.

As to claim 10, prior art does not show, "**the output dependent on the current flowing through the current sampling resistor is provided to the second amplifier for comparison with the stored output value, the second amplifier providing the data input line voltage**" in combination with other limitations of claim 10.

Response to Arguments

7. Applicant's arguments filed **May 13, 2008** have been fully considered but they are not persuasive.

On the 1st and 2nd page of Remarks, Applicant argues that **Holloman fails to teach any circuitry for providing one or more feedback signals representing the**

voltage drop across the resistor. The Examiner respectfully disagrees to this assertion. Holloman clearly teaches circuitry for providing feedback signals representing the voltage drop across the resistor (see figs. 1 and 2).

On the 3rd page of Remarks, Applicant asserts, **"… Holloman does not suggest … the gates of the address transistor and each sampling transistor are controlled by a shared address line**". The Examiner respectfully again disagrees to this statement. Holloman discloses that a device where the gates of the address transistor (fig. 1(12)) and each sampling transistor (fig. 1(32)) are controlled by a shared address line (figs. 1-4).

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Afroza Y. Chowdhury whose telephone number is 571-270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
8/16/2008
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